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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,141	06/27/2003	Jonathan M. Haswell	FIS920030157	1140

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,141	HASWELL ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response was received December 19,2005.

- Claims 1-20 stand rejected.
- Specification is now acceptable.
- Rejections under 35 USC 112 are withdrawn.
- Claim objection is withdrawn.

Application pending.

Response to Amendment

Applicants' arguments/amendments with respect to amended claims 1, 2, 11, 16 and 17 and previously presented claims 3-10, 12-15 and 18-20 filed December 19, 2005 have been received. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicants contend, "...Albonesi (prior art of record) does not disclose or suggest substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor..." The Examiner respectfully disagrees. Albonesi teaches (i.e., col. 8, lines 14-20) to detect a data error while data is transferred from the memory to the processor and generating corresponding corrected data if an error is detected in the original data. The Examiner would like to point out that, basically, claim 1 teaches to transmit data from a memory to the processor and check for errors in the data and if

there is an error then substitute another data to the processor. It is the Examiner's conclusion that this concept is not novel.

The Examiner disagrees with the Applicants and maintains rejections with respect to amended claims 1, 2, 11, 16 and 17 and previously presented claims 3-10, 12-15 and 18-20. All arguments have been considered. It is the Examiner's conclusion that amended claims 1, 2, 11, 16 and 17 and previously presented claims 3-10, 12-15 and 18-20, as presented, are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto (USPN 4617660) further in view of Albonesi (USPN 4920539).

As per claim 1, Sakamoto substantially teaches a faulty-memory processing method and apparatus in a data processing system which executes a time-sharing data process with breaks. Hard error which may exist in a cell in a normal memory is detected by using an error correction circuit. After correcting an error in information read out from a detected hard-error cell in the normal memory, information including the above corrected information with respect to the

detected hard-error cell is transcribed into a relief memory. The above correction and transcription is executed during the breaks in the time-sharing data process. Sakamoto teaches (Figure 1) a data processing system fundamentally has a CPU, a memory unit (MU), and data channel units (DCH), connected to each other by a common bus. Input/output (I/O) devices are coupled to the data channel units. The CPU performs data processing in cooperation with the MU. The DCH's control the I/O devices with respect to the MU. The MU includes an error detecting circuit for detecting errors in read and write data with respect to the MU and an error correcting circuit for automatically correcting the detected error. Sakamoto teaches (col. 11, lines 21-46) a faulty memory processing method in a data processing system including memory means having a normal memory with a plurality of cells for storing information, a relief memory, and error correction means for detecting and correcting an error in information read out from at least one cell in said normal memory, said data processing system executing a time-sharing data process with time period breaks, said faulty-memory processing method comprising the steps of: detecting a hard error which may exist in at least one cell in said normal memory, said detection being carried out using said error correction means; correcting, using said error correction means, an error in information read out from a detected hard error cell of the normal memory; transcribing information including the corrected information with respect to the detected hard-error cell of the normal memory into the relief memory, said correcting and transcribing steps being executed during the time period breaks in said time-sharing data process; and processing in a normal mode where data read out from the memory means are immediately utilized without waiting for the detection and correction performed by the error.

Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application.

However, Albonesi teaches, in an analogous art, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the checking of the data signal for corruption at the time it is received by the computer processor within the method and apparatus of Sakamoto. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by checking the data signal for corruption at the time it is received by the computer processor would have relieved the memory of such detection and correction process and hence enhanced the system.

As per claims 2, 12 and 17, Sakamoto substantially teaches (col. 4, lines 53-62), in view of above rejections, to determine if the corrupted data may be corrected.

As per claims 3, 5, 14 and 18, Sakamoto substantially teaches (Figure 4 and col. 5, lines 22-41), in view of above rejections, the computer processor or CPU to determine if the received signal is corrected.

As per claims 4 and 19, Sakamoto substantially teaches (Figure 5), in view of above rejections, the corrected data to be rewritten to the memory.

As per claims 6-7 and 13, Sakamoto substantially teaches (Figure 7 and associated text), in view of above rejections, for each memory element of a dynamic RAM, the refresh operation is periodically executed in response to the refresh timing signal S.sub.f. FIG. 7 indicates a memory cell array of a dynamic RAM of 256 K bit. In this RAM, all cells (1024 bits) in a column are simultaneously refreshed at an interval of 15 msec. All cells in the RAM (256 columns) will be refreshed in about 4 msec. As is known, in FIG. 7, if a refresh address (column address) of "2" and a row address of "3" are applied to the RAM, the contents in a cell 18 are read out.

As per claims 8-10 and 15, Albonesi substantially teaches, in view of above rejections, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and

destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field.

As per claim 11, Sakamoto substantially teaches a faulty-memory processing method and apparatus in a data processing system which executes a time-sharing data process with breaks. Hard error which may exist in a cell in a normal memory is detected by using an error correction circuit. After correcting an error in information read out from a detected hard-error cell in the normal memory, information including the above corrected information with respect to the detected hard-error cell is transcribed into a relief memory. The above correction and transcription is executed during the breaks in the time-sharing data process. Sakamoto teaches (Figure 1) a data processing system fundamentally has a CPU, a memory unit (MU), and data channel units (DCH), connected to each other by a common bus. Input/output (I/O) devices are coupled to the data channel units. The CPU performs data processing in cooperation with the MU. The DCH's control the I/O devices with respect to the MU. The MU includes an error detecting circuit for detecting errors in read and write data with respect to the MU and an error correcting circuit for automatically correcting the detected error. Sakamoto teaches (col. 11, lines 21-46) a faulty memory processing method in a data processing system including memory means having a normal memory with a plurality of cells for storing information, a relief memory, and error correction means for detecting and correcting an error in information read out from at least one cell in said normal memory, said data processing system executing a time-sharing data process with time period breaks, said faulty-memory processing method comprising the steps of: detecting a hard error which may exist in at least one cell in said normal memory, said detection

being carried out using said error correction means; correcting, using said error correction means, an error in information read out from a detected hard error cell of the normal memory; transcribing information including the corrected information with respect to the detected hard-error cell of the normal memory into the relief memory, said correcting and transcribing steps being executed during the time period breaks in said time-sharing data process; and processing in a normal mode where data read out from the memory means are immediately utilized without waiting for the detection and correction performed by the error.

Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application.

However, Albonesi teaches, in an analogous art, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the checking of the data

signal for corruption at the time it is received by the computer processor within the method and apparatus of Sakamoto. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by checking the data signal for corruption at the time it is received by the computer processor would have relieved the memory of such detection and correction process and hence enhanced the system.

As per claim 16, Sakamoto substantially teaches a faulty-memory processing method and apparatus in a data processing system which executes a time-sharing data process with breaks. Hard error which may exist in a cell in a normal memory is detected by using an error correction circuit. After correcting an error in information read out from a detected hard-error cell in the normal memory, information including the above corrected information with respect to the detected hard-error cell is transcribed into a relief memory. The above correction and transcription is executed during the breaks in the time-sharing data process. Sakamoto teaches (Figure 1) a data processing system fundamentally has a CPU, a memory unit (MU), and data channel units (DCH), connected to each other by a common bus. Input/output (I/O) devices are coupled to the data channel units. The CPU performs data processing in cooperation with the MU. The DCH's control the I/O devices with respect to the MU. The MU includes an error detecting circuit for detecting errors in read and write data with respect to the MU and an error correcting circuit for automatically correcting the detected error. Sakamoto teaches (col. 11, lines 21-46) a faulty memory processing method in a data processing system including memory means having a normal memory with a plurality of cells for storing information, a relief memory, and error correction means for detecting and correcting an error in information read out from at least one cell in said normal memory, said data processing system executing a time-sharing data

process with time period breaks, said faulty-memory processing method comprising the steps of: detecting a hard error which may exist in at least one cell in said normal memory, said detection being carried out using said error correction means; correcting, using said error correction means, an error in information read out from a detected hard error cell of the normal memory; transcribing information including the corrected information with respect to the detected hard-error cell of the normal memory into the relief memory, said correcting and transcribing steps being executed during the time period breaks in said time-sharing data process; and processing in a normal mode where data read out from the memory means are immediately utilized without waiting for the detection and correction performed by the error.

Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application.

However, Albonesi teaches, in an analogous art, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the

correct data corresponding to said address field. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the checking of the data signal for corruption at the time it is received by the computer processor within the method and apparatus of Sakamoto. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by checking the data signal for corruption at the time it is received by the computer processor would have relieved the memory of such detection and correction process and hence enhanced the system.

As per claim 20, Sakamoto substantially teaches, in view of above rejections, (col. 1, lines 14-32) a memory unit in a data processing system is provided with a function for detecting an error in data read from the memory unit and for correcting the detected error by an error correcting code (ECC).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
September 14, 2006

GUY LAMARRE
PRIMARY EXAMINER